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Description

IMPROVED BOND PAD

BACKGROUND OF INVENTION

[0001] Technical Field

[0002] The present invention relates generally to semiconductor devices, and more particularly, to the design of bond pads for wirebond interconnections.

[0003] Related Art

[0004] Wirebonding is commonly used to form an electrical interconnection between an integrated circuit and another device, e.g., lead frame, interposer, or printed circuit board. Attaching a wirebond to an active region of a chip consists of pressing a wirebond ball, having a conductive wire attached thereto, into a bond pad.

[0005] Before being used in a final product, or sent to an end user, the chip must be tested to ensure product reliability. Such testing may be performed on the chip before or after wirebonding, depending upon the design of the bond pad. A probing device is used to measure open or closed elec-

trical systems. During probing a probe tip contacts a surface of the bond pad to measure electrical conduction. There is often a layer of oxide, or "skin", on the surface of the bond pad that was created during formation of the bond pad. Therefore, sufficient down force is required when contacting the bond pad surface with the probe tip to penetrate the skin. Otherwise, erroneous readings may be produced, resulting in the discarding of functioning chips. Due to the downward force of the probe tip some of the bond pad material is removed during probing. As a result, the amount of bond pad material available for wirebonding is also reduced. Also, due to the uneven topography on the surface of the bond pad, the probe tip often gouges the bond pad material, leaving a pile up of bond pad material on the surface of the bond pad, and on the probe tip itself. The pile up of bond pad material on the surface of the bond pad may result in Kirkendal Voiding, wherein voids within the interconnection are produced during wirebonding as the excess bond pad material in the pile up is consumed by the wirebond ball. The excess bond pad material on the probe tip must also be cleaned frequently causing production delays.

[0006] By minimizing the amount of bond pad material, the

above-stated problems are reduced. There is, therefore, a process window for bond pad thickness that minimizes the amount of bond pad removal and pile up. For example, an optimal process window for thickness of the bond pad may be 300-800nm, e.g., 400nm, for tight pitch wirebond products, e.g., a pitch of less than 65nm, pitch referring to the width of the bond pad and the spacing between bond pads.

[0007] However, after the wirebond interconnection is formed some of the interconnections must withstand at least two mechanical tests, namely, a stud pull test and a ball shear test, to qualify the interconnection formation process for further use. The resistance of the interconnection to mechanical failure depends upon the pad thickness. In particular, the interconnection typically performs better during these tests as the amount of bond pad material is increased. Therefore, the process window for bond pad thickness during wirebond mechanical testing may be 800-1500nm, e.g., 1000nm, for a tight pitch wirebond product.

[0008] Clearly, there is a problem in forming a bond pad having sufficient bond pad material to pass the mechanical tests performed on the wirebond interconnection, and at the

same time minimize the amount of bond pad material to reduce the removal and pile up of bond pad material during probing.

[0009] Therefore, there is a need in the industry for a bond pad that overcomes the above problems

SUMMARY OF INVENTION

[0010] The present invention provides a bond pad upon which a wirebond interconnection is to be formed that solves the above-stated problems.

[0011] A first aspect of the invention provides a method of forming a bond pad for use in a wirebond interconnection, comprising: depositing a first layer of bond pad material on a substrate; and depositing a second layer of bond pad material on the first layer, wherein the first layer has a higher Young"s Modulous of Elasticity than the second layer.

[0012] A second aspect of the invention provides a method of forming a bond pad for use in a wirebond interconnection, comprising: depositing a first layer of bond pad material on a substrate; and depositing a second layer of bond pad material on the first layer, wherein a hardness of the first layer is greater than a hardness of the second layer.

[0013] A third aspect of the invention provides semiconductor

device, comprising: a first layer formed on a substrate; and a second layer on the first layer, wherein the first layer of the bond pad has a higher Young"s Modulous of Elasticity than the second layer.

[0014] The foregoing and other features and advantages of the invention will be apparent from the following more particular description of the embodiments of the invention.

Brief Description of Drawings

[0015] The embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:

[0016] Fig. 1 depicts a portion of an integrated circuit chip having a metallization level thereover;

[0017] Fig. 2 depicts the chip of Fig. 1 having an oxide layer thereover;

[0018] Fig. 3 depicts the chip of Fig. 2 having a via formed within the oxide layer;

[0019] Fig. 4 depicts the chip of Fig. 3 having a first bond pad layer formed within the via of the oxide layer;

[0020] Fig. 5 depicts the chip of Fig. 4 having a second bond pad layer formed over the first bond pad layer within the via of the oxide layer;

[0021] Fig. 6 depicts the chip of Fig. 5 having a final passivation

layer over the surface of the chip;

[0022] Fig. 7 depicts the chip of Fig. 6 during probe testing;

[0023] Fig. 8 depicts the chip of Fig. 7 having a wirebond ball pressed into the bond pad; and

[0024] Fig. 9 depicts the chip of Fig. 8 having a wirebond interconnection formed on the bond pad.

DETAILED DESCRIPTION

[0025] Although certain embodiments of the present invention will be shown and described in detail, it should be understood that various changes and modifications might be made without departing from the scope of the appended claims. The scope of the present invention will in no way be limited to the number of constituting components, the materials thereof, the shapes thereof, the relative arrangement thereof, etc. Although the drawings are intended to illustrate the present invention, the drawings are not necessarily drawn to scale.

[0026] Fig. 1 depicts a portion of a chip 10 typically used in integrated circuit devices. The portion of the chip 10 illustrated in Fig. 1 is the portion having the active circuitry therein. A metallization level 12 is formed over the surface of the chip 10 as is known in the art. The metalliza-

tion level 12 contains metal lines and vias 13, formed using processes known in the art. For ease of illustration, the metallization level 12 of the present example contains two metal lines and one via forming an electrical interconnection between the two metal lines. The metal lines and vias 13 within the metallization level 12 may consist of tantalum-nitride having a tantalum barrier surrounding the metal lines and vias 13, or copper or copper alloys having a barrier comprising titanium-nitride, or other hard refractory metal, when used on combination with a copper interconnect (described infra), or tungsten when used on combination with an aluminum interconnect.

[0027] As illustrated in Fig. 2, an oxide layer 14 is formed over the surface of the metallization level 12. The oxide layer 14 may be formed using a plasma oxide deposition process, a TEOS based chemical-vapor deposition (CVD) process, or a plasma assisted CVD oxide deposition process. The oxide layer 14 may comprise a dielectric material such as polyimide, silicon dioxide, silicon nitride, fluorine doped oxide, or other low-k dielectrics.

[0028] As illustrated in Fig. 3, a via 16 is formed within the oxide layer 14 in a region of the chip 10 where the metal lines 13 are located in order to make electrical interconnection

between the metal lines 13 of the metallization level 12 and the wirebond interconnection (formed infra). The via 16 is etched down to the surface of the metallization level 12, using a photolithography pattern and plasma etch process, or other similarly used processes.

[0029] As illustrated in Fig. 4, a first layer of a bond pad, or first bond pad layer 18 is deposited over at least a portion of the oxide layer 14. The first bond pad layer 18 conformally coats the via 16 within the oxide layer 14, and extends beyond the blueprint of the via 16. The first bond pad layer 18 may comprise $TiAl_x$, e.g., $TiAl_3$, or other aluminum alloys having at least 2% titanium, 2% copper, 2% silicon, 2% tungsten, or other similar material. The Young"s Modulous of Elasticity of the material selected for the first bond pad layer 18 is about 100 GPa, or greater and a hardness of about 0.8 or greater. The first bond pad layer 18 may be sputter deposited onto the surface of the oxide layer 14 using a plasma vapor deposition (PVD) technique, or other similar technique, to a thickness of about 100-800nm.

[0030] As illustrated in Fig. 5, a second layer of the bond pad, or second bond pad layer 20 is then deposited on the surface of the first bond pad layer 18, and may comprise alu-

minum, aluminum-copper alloys, aluminum-titanium alloys, or other similarly used materials. The second bond pad layer 20 is formed using a PVD process, or other similarly used process. The second bond pad layer 20 may be formed having a thickness of about 100-600nm. The first and second bond pad layers 18, 20 form a bond pad stack or bond pad 22, having a total thickness less than, or equal to 1200nm. It should be noted that the thickness of each of the first and second bond pad layers 18, 20 may be adjusted as needed. The bond pad 22 is electrically connected to the active region of the chip 10 through the metal lines and vias 13 within the metallization level 12. Customarily a bond pad comprises only a single layer of material, for example, primarily Al and its alloys. A single layer bond pad composed primarily of Al has a Young"s Modulous of Elasticity of about 88 GPa, or less than about 90 GPa, and a hardness of about 0.6 GPa. The present invention, however, replaces a portion of the conventional aluminum bond pad with the first bond pad layer 18 such that the total bond pad thickness required for a particular application is maintained, but the amount of aluminum is reduced. As mentioned above, the first bond pad layer 18 has a Young"s Modulous of Elasticity of about 100 GPa or

greater, and a hardness of about 0.8 GPa. The higher Young"s Modulous of Elasticity and hardness makes the first bond pad layer 18 more resistant to the probe testing than the second bond pad layer 20. As a result, less of the bond pad 22 is removed during probe testing, therefore, sufficient bond pad material is still present at the time of wirebonding. In addition, the Young"s Modulous of Elasticity of the first bond pad layer 18 increases the resistance of the wirebond interconnection (formed infra on the bond pad 22) to mechanical failure during mechanical tests performed on the wirebond interconnection.

[0031] Following formation of the bond pad 22 an oxide nitride layer 24 is deposited over the surface of the chip 10, using a CVD process, a plasma assisted CVD process, or other similarly used process (Fig. 6). Thereafter, a photosensitive polyimide (PSPI) resist layer 26 is deposited over the surface of the oxide nitride layer 24. The oxide nitride layer 24 and the PSPI layer 26, which together form a final passivation layer 28, are then cured. For example, the final passivation layer 28 is exposed to a temperature of about 350°C for about 1 hour and 30-45 minutes. The curing process causes the final passivation layer 28 to shrink from a thickness of about 12 microns to about 6

microns, thereby sealing the surface of the chip 10. The final passivation layer 28 serves to protect and insulate the chips 10 from damage during packaging and probe testing.

[0032] Thereafter, a via 30 is etched in the final passivation layer 28 down to the second layer 20 of the bond pad 22, using a photoetching process, or other similarly used process, to expose the bond pad 22 for probe testing and wire-bonding (described infra) (Fig. 7).

[0033] Fig. 7 illustrates the probe testing process performed on the bond pad 22. In particular, the probe tip 32 penetrates the second layer 20 of the bond pad 22. The first layer 18 of the bond pad 22, however, is hard enough to resist penetration by the probe tip 32. Because the probe tip 32 is unable to penetrate the first layer 18 of the bond pad 22 not as much of the bond pad material is removed, and pile up of bond pad material on the surface of the chip 10 and on the probe tip 32 is reduced. In fact, the first layer 18 of the bond pad 22 is not removed by the probe tip 32, and the portion of the second layer 20 that may be removed by the probe tip 32 is smaller it would have been had the entire bond pad 22 thickness been formed of the aluminum. As a result, less of the total

bond pad 22 is removed during probing. Additionally, because there is a reduced occurrence of pile up of removed bond pad material on the surface of the chip 10, the occurrence of Kirkendal Voiding (described supra), a known failure mechanism of the related art, is also reduced.

[0034] Thereafter, a wirebond or ball 34, having a wire 36 affixed thereto, is pressed onto the bond pad 22, as shown in Fig. 8. The ball 34 may comprise gold, or other similarly used material. The wire 36 may comprise copper, or other similarly used material. The ball 34 undergoes a thermal cycling process whereby in this example, at least a portion of the aluminum within the second bond pad layer 20 is consumed by the gold ball 34 forming an Au/Al intermetallic wirebond interconnection 38, as illustrated in Fig. 9. The interconnection 38 securely affixes the wire 36 to the bond pad 22 thereby providing electrical connection between a lead frame (not shown) and the chip 10.

[0035] Mechanical tests may be performed on the interconnection 38 to ensure stability of the interconnection 38 and qualify the formation process for further use. For example, a ball shear test and a stud pull test may be performed. During the ball shear test a force is applied to the interconnection 38 in the direction of arrow 40. The force

necessary to shear the interconnection 38 is measured. During the stud pull test an upward force, a force in the direction of arrow 42, is applied to the wire 36. The force required to break the interconnection 38 is measured.

[0036] As mentioned above, the bond pad 22 of the present invention is more resistant to removal of the bond pad material during probing. Accordingly, more of the bond pad 22 is present at the time of wirebond interconnection 38 formation. As a result, a better interconnection 38 is formed, therefore, a greater force is needed to break the interconnection 38 during the ball shear test and the stud pull test. Additionally, the material selected for the first layer 18 of the bond pad 22 has a higher Young"s Modulous of Elasticity and hardness than the aluminum in the second layer 20. This also increases the resistance of the bond pad 22 and the interconnection 38 to the forces applied to the interconnection 38 during the mechanical tests. Furthermore, because the bond pad 22 is more resistant to removal during probe testing, there is less excess bond pad material on the probe tip. This reduces the necessity to clean the probe tip as frequently, thereby minimizing production delays.